amended paragraph.

A7

--**Figure 25**, which is presented on two separate sheets labeled **Figure 25A** and **25B**, illustrates one example of a KLFM process.--

IN THE CLAIMS

Please cancel claims 1-3, 14-42, and 65-87.

Please amend claims 4 and 43 as follows:

A8

4. (Amended) For an electronic design automation application, a method of placing circuit modules in an integrated circuit ("IC") layout, wherein the IC layout has a number of circuit elements, a net having a set of circuit elements, the method comprising:

using a diagonal line to measure a placement metric;

wherein using the diagonal line to measure a placement metric comprises calculating an estimate of the length of interconnect lines necessary to connect the circuit elements of said net, wherein the calculation measures the length of at least one line that is at least partially diagonal.

A9

43. (Amended) For an electronic design automation application, a method of placing circuit modules in an integrated circuit ("IC") layout, wherein said IC layout includes a net and a plurality of circuit elements, wherein the net represents interconnections between a set of circuit elements, the method comprising:

constructing a connection graph that models the topology of interconnect lines for connecting the circuit elements of the net, said connection graph having edges, each edge connecting two circuit elements of the net, wherein at least one of the edges is at least partially diagonal;

identifying a placement metric based on the connection graph.

Please add claims 88-96.

--88. (New) A method of placing circuit modules in an integrated circuit ("IC") layout, wherein said IC layout includes a set of circuit elements, the method comprising:

a) identifying a connection graph that models the topology of interconnect lines for connecting the set of circuit elements, wherein said connection graph has a plurality of edges, wherein at least some of the edges are neither parallel nor orthogonal to each other,

b) identifying a placement metric based on the connection graph.

89. (New) The method of claim 88, wherein identifying a placement metric comprises calculating the length of the graph.

90. (New) The method of claim 89, wherein the length provides an estimate of interconnect-line length needed to connect the circuit elements of the net.

91. (New) The method of claim 90, wherein said placement metric estimate is identified to obtain a placement cost of an initial placement configuration.

92. (New) The method of claim 90, wherein said placement metric estimate is identified to obtain a placement cost of a modified placement configuration.

93. (New) The method of clam 88, wherein the edges that are neither parallel nor orthogonal forms a 45° angle with respect to each other.

94. (New) The method of clam 88, wherein the edges that are neither parallel nor orthogonal forms a 120° angle with respect to each other.

95. (New) The method of claim 88, wherein the connection graph is a minimum spanning tree.

96. (New) The method of claim 88, wherein the connection graph is a Steiner tree.--

REMARKS

Reconsideration of the patent application in view of the preceding amendments and the following remarks is respectfully requested.